This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

OIPE JC34
JAN 1 2 2004
PATENT & TRADEMARK OFFICE

Docket No.: M4065.0139/P139-A
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Cem Basceri

Confirmation No.: 2413

Application No.: 09/633,132

Group Art Unit: 2815

Filed: August 4, 2000

Examiner: E. Lee

For: METHOD FOR IMPROVING THE SIDEWALL STOICHIOMETRY OF THIN FILM CAPACITORS

DECLARATION OF GARO DERDERIAN UNDER 37 C.F.R. § 1.132

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Garo Derderian, hereby declare as follows:

RECEIVED
JAN 20 2004
TECHNOLOGY CENTER 2800

1. I am of legal age and under no disability that prevents me from attesting to the following statements and information which are based on my personal knowledge and observations.

2. I currently reside at 6184 S. Schooner Place, Boise, ID 83716.

3. I am currently employed by Micron Technology, Inc. as a Senior Engineer. I have been employed by Micron Technology, Inc. as a Process Development Engineer since May 1995. Previously, I was employed by the University of California, Irvine (UCI) for three years (1991-1994) as a Research Assistant in the Materials Science Department.

4. I have a Master of Science degree in Materials Science and Engineering from UCLA (received 1989), and a Doctoral degree in Materials Science and Engineering from UCI (received 1995).

5. From May 1995 to the present, I have been engaged in the research and development of film deposition and film treatment processes used in semiconductor manufacturing. In particular, I have been involved in various developmental projects regarding the chemical vapor deposition (CVD) of metals and oxides, including high constant dielectrics for DRAM manufacturing. As a result, I have knowledge of the chemical vapor deposition of thin films.

6. During my research and development of film deposition and film treatment, I have had at least three years experience in conventional sputtering techniques, including forming thin film materials by these methods.

7. Additionally, during my training as a materials scientist, after earning my Masters Degree, I had at least three years of experience in wet-techniques; specifically, spin-coating sol-gel materials onto substrates. As a result, I have knowledge of the spin-coat depositions of thin films.

8. I have read and understand the above-captioned application (the '132 application) and the pending claims as amended (the "Claimed Invention"), as well as the Office Action dated August 11, 2003.

9. I understand that claims 39 and 41-46 of the '132 application are under final rejection by the U.S. Patent and Trademark Office under §103(a) as being unpatentable over Laibowitz et al., U.S. Patent No. 6,088,216 (hereinafter "Laibowitz"), in view of Azuma et al., U.S. Patent No. 5,516,363 (hereinafter "Azuma").

10. I understand that claims 48 and 50-55 of the '132 application are under final rejection under §103(a) as being unpatentable over Laibowitz, in view of Azuma, and further in view of Leung et al., U.S. Patent No. 5,563,762 (hereinafter "Leung").

11. I also understand that claims 74-83 of the '132 application are also under final rejection under §103(a) as being unpatentable over Hosotani et al., U.S. Patent No. 6,051,859 (hereinafter "Hosotani") in view of Azuma.

12. Because of my background, I believe that as of the filing date of the '132 application, and indeed as of today, a person having ordinary skill in the art of deposition of metals by CVD would be a person with at least a Masters degree in Materials Science and Engineering and with at least three (3) years processing experience in the deposition processes of the semiconductor industry. I am knowledgeable as to what such a person of ordinary skill in the art would have known and understood relating to the deposition of CVD metals in semiconductor processing as of August 2000.

13. Because of my background, I believe that as of the filing date of the '132 application, and indeed as of today, a person having ordinary skill in the art of deposition of metals by conventional sputtering techniques would be a person with at least a Masters degree in Materials Science and Engineering and with at least three (3) years processing experience in the deposition processes of the semiconductor industry. I am knowledgeable as to what such a person of ordinary skill in the art would have known and understood relating to the deposition of metals by conventional sputtering techniques in semiconductor processing as of August 2000.

14. Because of my background, I believe that as of the filing date of the '132 application, and indeed as of today, a person having ordinary skill in the art of depositing metals by "wet-techniques" would be a person with at least a Masters degree in Materials Science and Engineering and with at least three (3) years processing experience in the deposition processes of the semiconductor industry. I am knowledgeable as to what such a person of ordinary skill in the art would have known and understood relating to the spin-coating deposition of metals in semiconductor processing as of August 2000.

15. It is well known in the art that metal oxides and high dielectric constant materials comprise materials of the general form ABO_3, wherein A and B are cations. The term is intended to include materials of the form $A'A''BO_3$, $AB'B''O_3$, and $A'A''B'B''O_3$, wherein A', A'', B', and B'' are different metal elements. Preferably, A, A', and A'' are metals selected from the group comprising Ba, Bi, Sr, Pb, Ca, and La. B, B', and B'' are preferably selected from the group comprising Ti, Zr, Ta, Mo, W, and Nb.

16. One example of a high dielectric constant material is barium strontium titanate ($(Ba, Sr)TiO_3$) (BST). Typically, it is ideal to have the barium (Ba) to strontium (Sr) ratio of approximately 70 to 30, respectively. The 70:30 ratio allows the high dielectric constant material to operate in the paraelectric region for DRAM applications. Additionally, it is important that the titanium (Ti) percentage of the high dielectric constant material be between approximately 50% to approximately 53.5%. If the percentage of Ti is outside the given range, the BST will exhibit poor physical and electrical properties. For example, a high dielectric constant material having a Ti percentage outside of the given range will exhibit increased current leakage, which will lead to poor performance of the DRAM cell of which it is a part.

17. Because the ratio between Ba and Sr should be approximately 70:30, and the Ti percentage should be in a range from approximately 50% to approximately 53.5%, it is important that the high dielectric constant material have the given stoichiometry. Other examples of high dielectric constant materials include lead zirconate titanate ($PbZr_xTi_YO_3$) (PZT), barium titanate ($BaTiO_3$), and strontium titanate ($SrTiO_3$). Each of the foregoing compounds also requires its own stoichiometry, with a Ti percentage in the range of approximately 50% to approximately 53.5%.

18. Although it has been recognized that homogenous stoichiometry is important in the formation of high dielectric constant materials, it is my understanding that those skilled in the art find it difficult to maintain the stoichiometry of the high dielectric materials once deposited on a substrate to create a thin film, as discussed in further detail below.

19. Turning now to the '132 application, the invention improves on the inhomogeneity achieved by conventional techniques by ion implantation. By ion implanting the dopants comprising the high dielectric material, e.g., Ba, Sr, and Ti, one may ensure that the stoichiometry of the high dielectric material is uniform when forming a thin film.

20. I have been asked to review the references cited by the Office Action and determine whether one of ordinary skill in the art would combine the aforementioned references, and if that combination would demonstrate the obviousness of the invention.

21. I have been provided and read the Laibowitz, Azuma, Leung, and Hosotani patents. It is my understanding that Laibowitz discloses a three-dimensional (3D) DRAM capacitor comprising a substrate 12, whereupon a mesa 51 and high dielectric film 56 are formed (Figure 7). Laibowitz does not disclose a capacitor in which the stoichiometry of the high dielectric constant thin film material is substantially uniform on a sidewall region. It is my understanding that Laibowitz uses deposition techniques upon which the '132 application improves. For example, Laibowitz discloses a "[h]igh dielectric constant material 66 [] *deposited* to form dielectric layer 67 having a predetermined thickness…." (Col. 3, lines 43-45) (emphasis added). Although Laibowitz fails to state which deposition technique it uses to deposit the high dielectric constant material, it is well known in the art that these materials are generally deposited by conventional techniques, such as sputtering or chemical vapor deposition (CVD).

22. It is my understanding that CVD techniques of depositing dielectric layer 56 of Laibowitz on a sidewall would not result in a capacitor in which the stoichiometry of the sidewalls is substantially uniform because CVD techniques suffer from inhomogeneity in stoichiometry on sidewalls of 3D structures.

23. It is my understanding that the same holds true for conventional sputtering techniques. Specifically, conventional sputtering techniques typically result in clumped areas of massed materials having non-uniform thicknesses and stratified layers that are improperly mixed to non-homogenous, i.e., non-uniform, proportions that are incapable of forming proper average crystals on sidewalls of either trenches or studs.

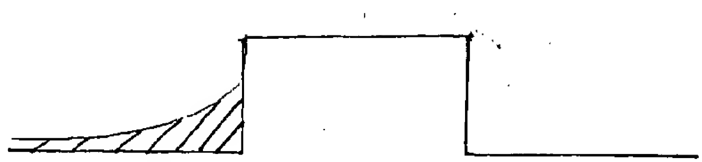
24. Because conventional techniques fail to form high dielectric constant thin films having uniform stoichiometry, I believe the stoichiometry of the deposited dielectric layer 56 of Laibowitz would not be substantially uniform on the sidewall regions.

25. It is my understanding that Azuma relates to a method of adding A or B-site dopants in precursor liquids to achieve homogeneity in said precursor liquid. Specifically, Azuma teaches doping "liquid precursor solutions for use in processes for forming thin-layer capacitors." (Abstract). The doped precursor solution is applied to a substrate, "conducted by dropping the precursor solution onto substrate 18 and then spinning substrate 18 at about 1500 RPM (the preferred range is about 1500-2000 RPM) for about 30 seconds." (Col. 18, lines 4-8). Azuma does not disclose that its "spin coat" method could be used on three-dimensional (3D) material layers.

26. It is illogical and unworkable to combine the process of Azuma with any 3D structure, including that of Laibowitz, for several reasons. First, performing a spin-coating deposition of high dielectric constant thin film on a substrate having a trench, would not result in a thin film material having a continuous layer on the sidewall regions and bottom. I have been provided illustrations of what may occur if a spin-coat were to be applied to a 3D substrate. I understand that FIGS. A and B were submitted with a response to a prior Office Action on May 22, 2003. It is my understanding, based on my experience with spin-coat techniques, that these illustrations are examples of what may occur if a spin-coat deposition process were applied to a 3D substrate, given the right parameters such as viscosity of the solution and the temperature at which the solution is applied.

27. Specifically, in a stud configuration, FIG. A for example, the high dielectric constant thin film precursor would accumulate at a bottom corner of one side of the illustrated stud, and not be able to coat the second opposite sidewall region.

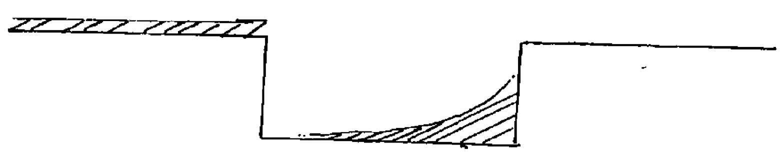
FIG. A.



(STUD)

28. In a trench configuration, for example FIG. B, the high dielectric constant thin film precursor would similarly accumulate at a bottom corner of one side of the trench, and not be able to coat the second opposite sidewall region.

FIG. B



(TRENCH)

29. Additionally, the process of spin-coating the high dielectric constant thin film precursor would result in an unworkable capacitor because the failure to achieve 100% step

coverage by spin-coating would open the circuit in which the capacitor is a part since there is a discontinuous layer.

30. Second, the precursor solution that is disclosed by Azuma cannot be deposited by either conventional sputtering or CVD techniques. It is well known in the art that solutions cannot be deposited using conventional sputtering techniques.

31. Similarly, Azuma's precursor solution cannot be deposited by CVD techniques. The precursor solutions, like many solutions used in wet-techniques, are formed by mixing high constant dielectric thin film materials with solvents to make an aqueous solution. Because the solvent typically has a higher vapor pressure as compared with the high dielectric constant thin film materials, it is not practical to deposit the Azuma liquid precursor by CVD. Because the vapor pressure of the high dielectric materials is low, while the vapor pressure of the solvents is high, the solvents would first vaporize leaving the high dielectric thin film materials behind. In addition, the temperature with which to vaporize the precursors would be too great for the high dielectric constant materials resulting in their decomposition. Therefore, the Azuma precursor solution could not be deposited by CVD. Even if it were to be deposited by CVD, the resulting structure would not have substantially uniform stoichiometry on the sidewall regions of a 3D substrate, as discussed above.

32. Moreover, spin-coat techniques are problematic in achieving thin films that are suitable for 3D DRAM capacitors, which require much thinner thin films than do flat capacitors. Flat capacitors, such as that disclosed by Azuma, typically have thin films in the range of approximately 1400/ to approximately 2000/. For example, Table 5 of Azuma describes a range of dielectric thicknesses from 1440/ to 1840/. 3D capacitors require significantly thinner thin films; typically requiring a dielectric thin film less than 100/. For example, Laibowitz discusses a DRAM circuit in development that "uses a trench capacitor" having a dielectric thin film, wherein "[t]he dielectric thickness is about 7 nm," or 70/. (Col. 1, lines 19-23). Wet-techniques, such as the spin-coating technique of Azuma, often achieve minimal thicknesses of only a few hundred angstroms (e.g., 500/), one order of magnitude greater than the thicknesses required by 3D capacitors. It is my understanding that one of skill in the art would not combine the spin-

coating technique with 3D structures, such as the Laibowitz capacitor, because the wet-technique cannot achieve the minimal thicknesses required by the 3D structure of Laibowitz.

33. Finally, there are density problems that arise with wet-techniques, such as the spin-coating disclosed by Azuma. Specifically, wet-techniques fail to achieve uniform densities, oftentimes creating pinholes or pores in the layers which they provide. Because the high dielectric constant materials are carried in liquid precursor solutions by adding solvents, heat must be applied to the substrate after the precursors have been spin-coat as to remove the solvent from the surface of the substrate. After removing the solvent, however, pinholes are created, leaving uneven densities of high dielectric constant thin film material on the substrate. A means of creating more uniform densities has been to apply several coats of a liquid precursor, and heating the substrate in between each coat.

34. The process of coating and heating achieves a more uniform density of the high dielectric thin film material, but also increases the thickness of the layer. Therefore, the failure of wet-techniques to achieve uniform densities on <u>flat</u> surfaces at minimal thicknesses is greatly exaggerated when using wet-techniques on 3D structures, such as the FIG. 7 Laibowitz 3D structure. Thus, it is my understanding that those skilled in the art would <u>not</u> combine the subject matter of the two references cited by the Office Action, because it is illogical and unworkable.

35. Additionally, it is my understanding that Hosotani, like Laibowitz, uses conventional techniques in forming its capacitor. Indeed, Hosotani admits that its "dielectric film is anomalously grown by the CVD method," (see col. 11, lines 64-65) lending support to my understanding that conventional techniques of forming a high dielectric constant thin film material fail to achieve good step coverage and also fail to provide homogenous stoichiometry.

36. Hosotani, like Laibowitz, does indeed show a 3D capacitor in FIG. 7, as the Office Action asserts. However, as discussed above with respect to claim 39, it is illogical and unworkable to combine Azuma with a 3D capacitor such as the capacitor disclosed by Hosotani.

37. I declare further that all statements made herein of my own knowledge are true and that all the statements made on information and belief are believed to be true; and further

Application No.: 09/633,132 Docket No.: M4065.0139/P139-A

that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and that such willful false statements may jeopardize the validity of the subject application or any patent issuing thereon. Further the Declarant sayeth not.

Dated: January 12, 2004

Respectfully submitted,

By [signature]
Garo Derderian

1714685 v1: 10R1L01!.DOC